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(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**
13500 North Central Expressway
Dallas Texas 75265(US)

(72) Inventor: **Gunturi, Sarma S.**
1403 Stoneboro
Richardson, Texas 75082(US)
Inventor: **Kleinert, Christian**
2512 Belmont Place
Plano, Texas 75023(US)

(74) Representative: **Leiser, Gottfried, Dipl.-Ing. et al**
Patentanwälte Prinz, Leiser, Bunke & Partner
Manzingerweg 7
W-8000 München 60(DE)

(54) Local interconnect using a material comprising tungsten.

(57) A tungsten silicide interconnect (28) is formed on device (10) as a local interconnect between devices. The tungsten silicide interconnect (28) provides several advantages over prior art methods, such as titanium nitride or polysilicon local interconnects.

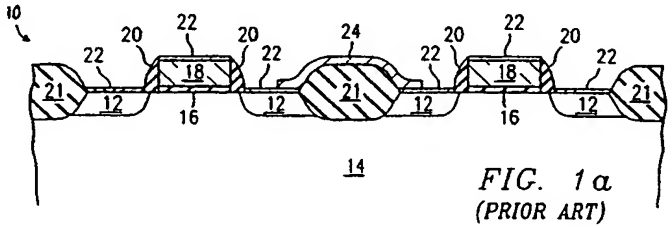

FIG. 1a
(PRIOR ART)

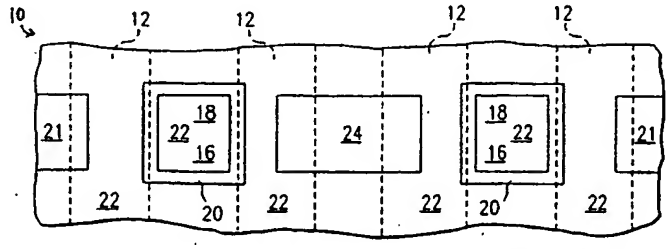

FIG. 1b
(PRIOR ART)

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gate N-junction sheet resistances to less than 1 ohm per square. A layer of titanium is disposed over the surface of the device, and a reaction between the titanium and silicon is performed in a nitrogen ambient at approximately 675°C. This reaction creates a titanium silicide layer 22 over the silicon and polysilicon portions of the device 10. The unreacted portions of the titanium layer on top of the oxide and over the titanium silicide layer 22 becomes TiN.

To form the TiN local interconnect 24, the device is patterned with photoresist after the titanium reaction step, and the resist is hardened using a high temperature bake and deep UV exposure. The TiN layer is then etched using a dry/wet etch comprising a fluorine-based dry etch and a $NH_4OH + H_2O_2 + H_2O$ wet etch.

Unfortunately, the procedure for etching the TiN to form the interconnects is not particularly selective to the silicon, polysilicon and titanium silicide portions of the device 10. Hence, in forming the interconnects, it is very possible that the device will be damaged. Further, the titanium silicide layer 22 is subject to peeling after the wet etch used to form the interconnect structure.

FIGUREs 2 and 3 illustrate cross-sectional side views of the present invention after first and second processing stages, respectively. While the invention is shown using the MOS interconnect structure of FIGUREs 1a-b, it may be used with any integrated circuit architecture, such as bipolar, etc.

In FIGURE 2, the gates 18, diffused regions 12, sidewall oxides 20, gate oxide 16 and field oxide regions 21 are formed as discussed in connection with FIGUREs 1a-b. Optionally, the diffused regions 12 and gates 18 may be silicided, thereby forming $TiSi_2$ layers 22 (not shown). After silicidation, if any, the TiN by-product is stripped.

In FIGURE 3, a thin layer of tungsten silicide (WSi_x) is deposited over the polysilicon gate layer after the sidewall oxide process has been completed. Typically, the deposited WSi_x layer comprises a ratio of 2.5:1 (W:Si). During subsequent processing, however, the ratio may vary dependent upon the high temperature cycles employed.

The deposited tungsten silicide layer is patterned and etched using a fluorine-based chemistry to form the local interconnect 28. The thickness of the tungsten silicide will depend upon the application and the desired resistance. Experimentally, a thickness of 3200 Angstroms has been used. The tungsten silicide layer may be etched using a well-established fluorine-based dry etch process. For example, SF_6 and Freon-114 may be used to etch the tungsten silicide layer to form the interconnect.

The tungsten silicide interconnect provides several advantages over the prior art. The fluorine-based dry etch process is highly selective to silicon, polysilicon and titanium silicide, and therefore will not damage the device during formation of the local interconnect. Further, tungsten silicide has a resistance of approximately 2-10 ohms per square, which compares favorably with titanium nitride and polysilicon. Further, the resistivity of the interconnect can be varied during processing by controlling the tungsten/silicon ratio.

It should be noted, that whereas the tungsten silicide local interconnect 28 has been shown connecting two diffused regions, it could be used in any situation where a local interconnect is desired.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

Claims

1. A method of forming a local interconnect structure on an integrated circuit structure, comprising the steps of:
   defining a local interconnect structure between two normally isolated areas of the integrated circuit; and
   forming the local interconnect structure using a material comprising tungsten.

2. The method of Claim 1 wherein said forming step comprises the steps of:
   forming a layer comprising tungsten on the surface of the integrated circuit structure; and
   removing portions of the layer to form the local interconnect structure on the integrated circuit structure.

3. The method of Claim 2 wherein said layer forming step comprises the step of depositing a layer comprising tungsten on the integrated circuit structure.

4. The method of Claim 3 wherein said depositing step comprises the step of depositing a tungsten and silicon compound.

5. The method of Claim 2 wherein said removing step comprises the step of etching the layer with an fluorine based etchant.

6. The method of Claim 5 wherein said removing step comprises the step of etching the layer with an etchant comprising SF_6.

7. The method of Claim 6 wherein said etching step comprises the step of etching the layer with and etchant comprising SF_6 and Freon-

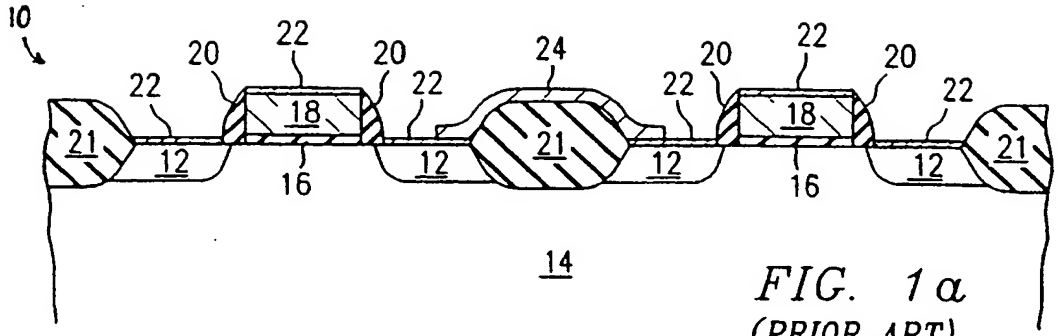

FIG. 1a
(PRIOR ART)

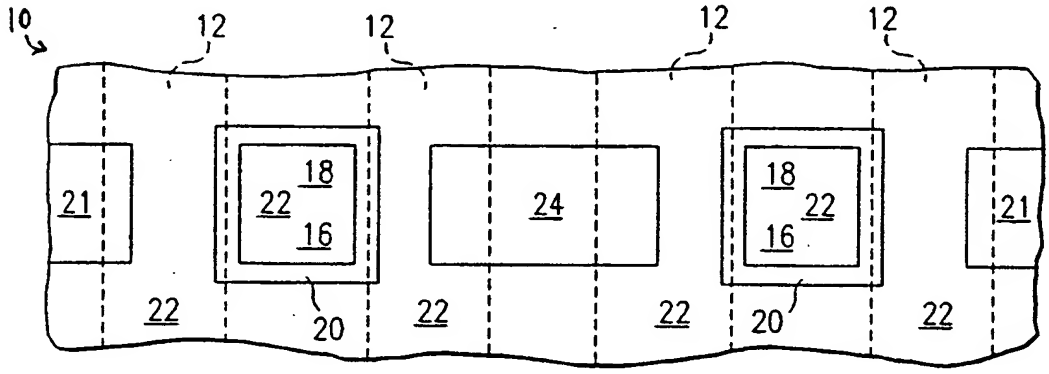

FIG. 1b
(PRIOR ART)

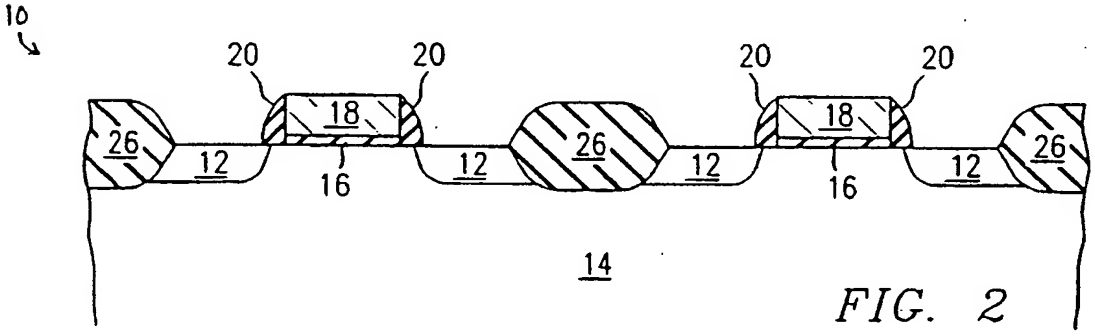

FIG. 2

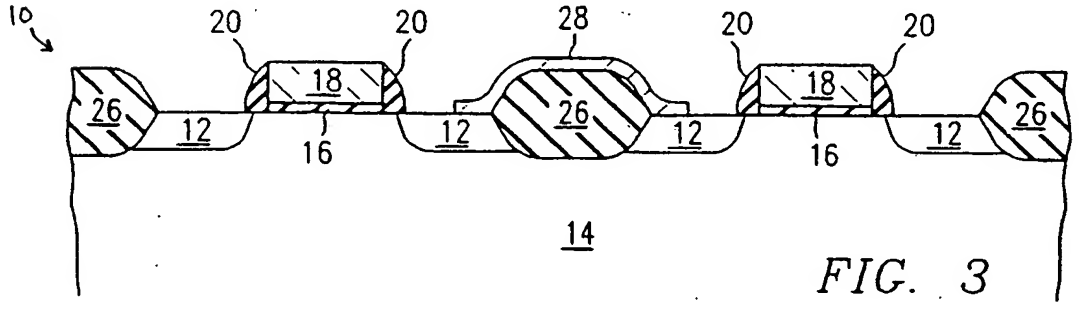

FIG. 3

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(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**
13500 North Central Expressway
Dallas Texas 75265(US)

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1403 Stoneboro
Richardson, Texas 75082(US)
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2512 Belmont Place
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Patentanwälte Prinz, Leiser, Bunke & Partner
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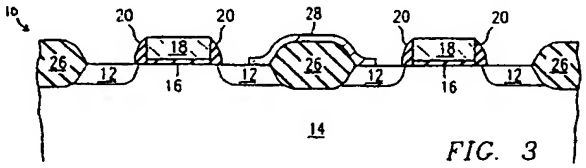

FIG. 3

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 10 8472

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	IEEE TRANSACTIONS ON ELECTRON DEVICES. vol. ED-34, no. 3, March 1987, NEW YORK US pages 682 - 688; Thomas E. TANG et al.: "Titanium Nitride local interconnect technology for VLSI" * figures 6a-c, 8 *	14,16	
X,A	DE-A-3 027 954 (SIEMENS AG.) * page 6, line 27 - page 7, line 31; claims 1, 2, 4, 5, 7; figures 1-3 *	1-4,15, 17,9-11	
X,A	EP-A-0 158 559 (COMMISSARIAT A L'ENERGIE ATOMIQUE) * page 1, lines 1 - 12 * * page 5, line 8 - page 8, line 26; figures 2-4 * * page 10, lines 15 - 34 *	1,15,17,2, 3,9,10	
X,A	IEDM TECHNICAL DIGEST 11 December 1988, SAN FRANCISCO, CA. pages 450 - 453; V.V. LEE et al.: "A selective CVD Tungsten local interconnect technology" * page 450, right-hand column - page 451, left-hand column; figures 1-4 *	1,15,17,9, 10,13	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
Berlin	03 January 92	KLOPFENSTEIN P R

CATEGORY OF CITED DOCUMENTS

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